# RV1126_RV1109_BATTERY_IPC_SMARTBELL_REF_V11

## Quick start solution

| RV1126_RV1109 Main difference | | |
|---|---|---|
| | RV1126 | RV1109 |
| CPU | Quad A7 | Dual A7 |
| NPU | 2.0Tops | 1.2Tops |
| ISP | 14M Pixel | 5M Pixel |

| Reference Design Main Functions Introduction | |
|---|---|
| Power | Discrete Power |
| RAM | EMMC/SLC NAND FLASH/SPI FLASH |
| ROM | DDR3L/DDR3/LPDDR3/LPDDR4 |
| Interface | SDMMC/SDIO/CIF/MIPI_DSI/MIPI_CSI0/ MIPI_CSI1/I2S/USB/ADC |



| | | | | | |
|---|---|---|---|---|---|
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| Project: | RV1126_REF | | | | |
| File: | 00.Cover Page | | | | |
| Date: | Tuesday, September 26, 2023 | | | Rev: | V1.1 |
| Designed by: | Yanhong.Li | Reviewed by: | <Checker> | Sheet: | 1 of 34 |

# Index and Notes

## Table of Content



## Note

**NOTE 1:**
**Component parameter description**
**1. DNP stands for component not mounted temporarily**
**2. If Value or option is DNP, which means the area is reserved without being mounted**

**NOTE 2:**
**Please use our recommended components to avoid too many changes.**
**For more informations about the second source,please refer to our AVL.**

## Generate Bill of Materials

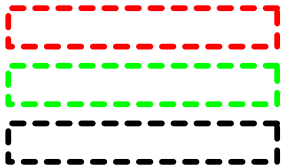
**Header:**

*Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption*

**Combined property string:**

*{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}*

## Graphic Description






| | | | | | |
|---|---|---|---|---|---|
| Rockchip 瑞芯微电子 | Rockchip Electronics Co., Ltd | | | | |
| Project: | RV1126_REF | | | | |
| File: | 01.Index and Notes | | | | |
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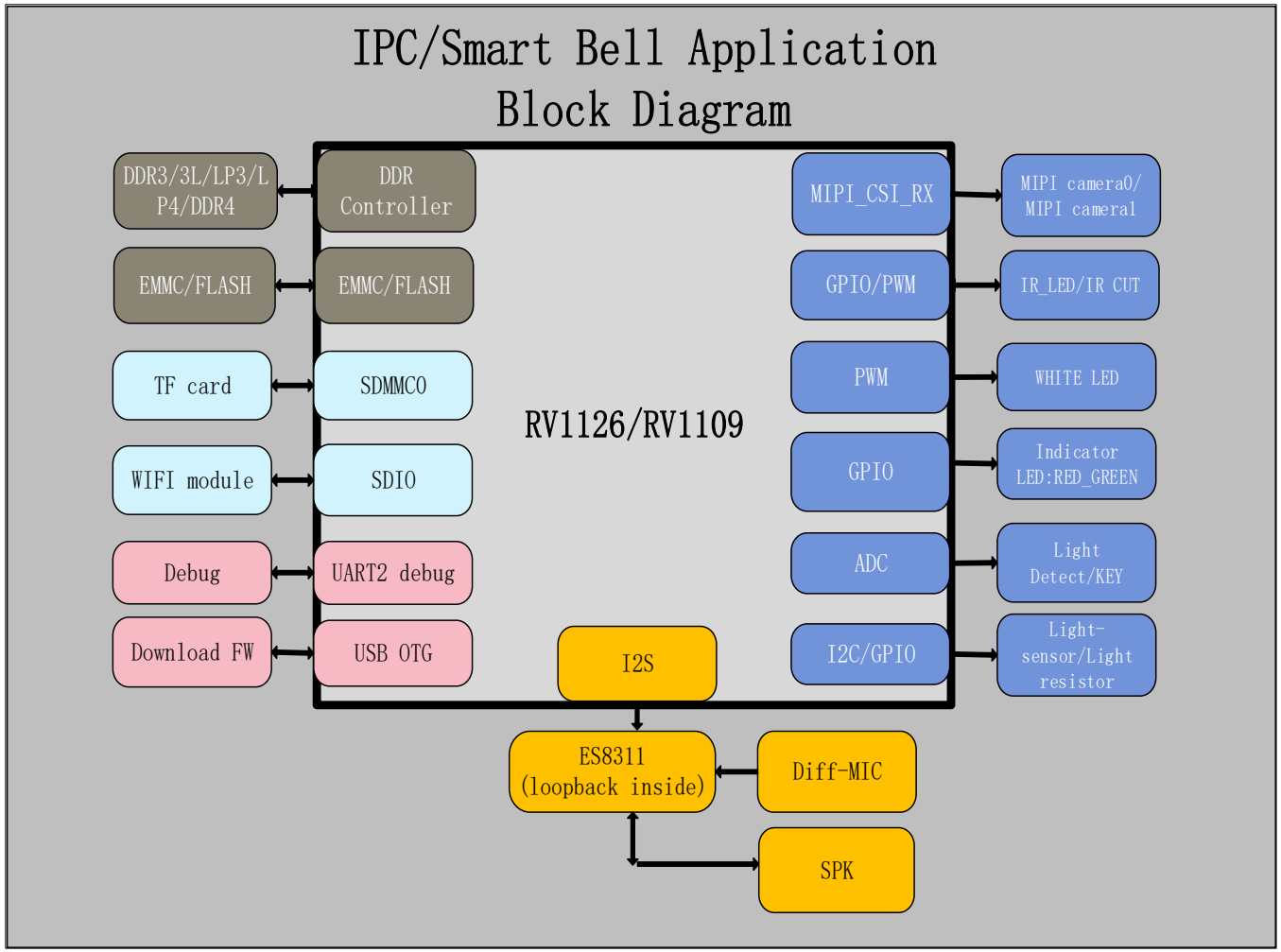
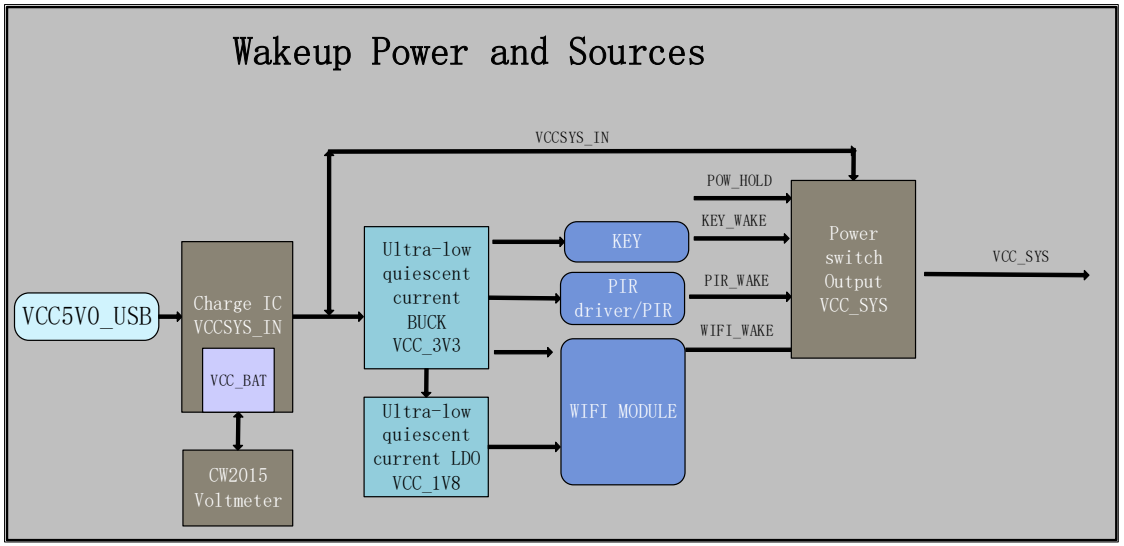
| Designed by: | Yanhong.Li | Reviewed by: | <Checker> | Sheet: | 2 of 34 |

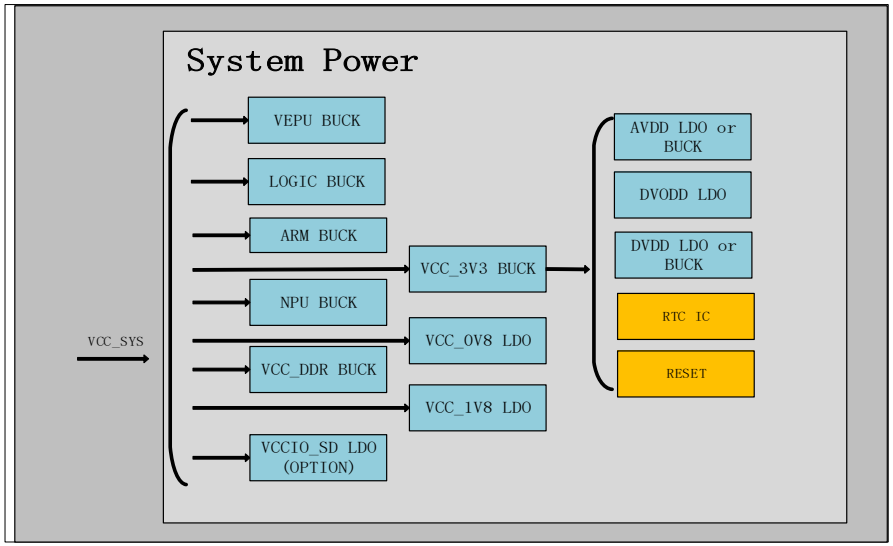
# Revision History

| Version | Date | Author | Change Note | Approved |
|---|---|---|---|---|
| V1.0 | 2020.07.13 | Liyh | RV1126_RV1109_BATTERY_IPC_SMARTBELL_REF_V10 | |
| V1.1 | 2020.09.28 | Liyh | RV1126_RV1109_BATTERY_IPC_SMARTBELL_REF_V11<br>Update:<br>1. For saving power consumption, NPU and VEPU are supplied separately.<br>2. For saving power consumption, the AVDD and DVDD of the camera module are powered by DCDC instead of LDO.<br>3. The change of audio :<br>Es8311 can support the loop-back function, so the hardware loop-back circuit can be deleted and the single ended MIC can be change to the difference mic. | |
| | | | | |




| | | | | | |
|---|---|---|---|---|---|
| Rockchip 瑞芯微电子 | Rockchip Electronics Co., Ltd | | | | |
| Project: | RV1126_REF | | | | |
| File: | 03.Block Diagram | | | | |
| Date: | Tuesday, September 26, 2023 | | | Rev: | V1.1 |
| Designed by: | Yanhong.Li | Reviewed by: | <Checker> | Sheet: | 4 of 34 |




# The reference power on sequence of discrete power

| Power Name | Power Channel | Time Slot | Default voltage | Supply Limit | Peak Current |
|---|---|---|---|---|---|
| VCC_0V8 | LDO | Slot: 1 | 0.8V | 0.5A | |
| VDD_LOGIC | BUCK | Slot: 2 | 0.8V | 2.0A | 1.75A |
| VDD_ARM | BUCK | Slot: 2 | 0.8V | 1.0A | 0.73A |
| VDD_NPU | BUCK | Slot: 2 | 0.8V | 3.0A | 2.11A |
| VDD_VEPU | BUCK | Slot: 2 | 0.8V | 2.0A | 1.0A |
| VCC_1V8 | LDO | Slot: 3 | 1.8V | 2.0A | |
| VCC_DDR | BUCK | Slot: 4 | 1.2V | 0.4A | |
| VCC_3V3 | BUCK | Slot: 5 | 3.3V | 2.0A | |
| VCC1V8_DOVDD | LDO | | 1.8V | 0.5A | |
| VCC1V2_DVDD | BUCK | | 1.2V | 0.5A | |
| VCC2V8_AVDD | BUCK | | 2.8V | 0.5A | |
| RESET | | | | | |

NOTE:VCC_DVDD and VCC_AVDD according to camera sensor voltage

| | | | | | |
|---|---|---|---|---|---|
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| Project: | RV1126_REF | | | | |
| File: | 04.Power Sequence | | | | |
| Date: | Tuesday, September 26, 2023 | | | Rev: | V1.1 |
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# I2C MAP

| Port | Bus Name | Domain | Pull-up voltage | Slave Device | Slave Addr (MS 7Bits) | Slave Bus Capability | Note |
|---|---|---|---|---|---|---|---|
| I2C0 | I2C0_SCL<br>I2C0_SDA | PMUIO1 | VCC_3V3 | HYM8563 | | | |
| | | | | CW2015 | | | |
| I2C1 | I2C1_SCL<br>I2C1_SDA | VCCIO4 | VCC_1V8 | MIPI Camera | | | |
| | | | | CIF Camera | | | |
| I2C4 | I2C4_SCL_M1<br>I2C4_SDA_M1 | VCCIO7 | VCC_3V3 | ES8311 | 0x18 | | |
| I2C5 | I2C5_SCL_M0<br>I2C5_SDA_M0 | VCCIO5_VDD | VCC_3V3 | CM32181A3OP | 0x48 | | |



| | | | | | |
|---|---|---|---|---|---|
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| File: | 05.I2C MAP | | | | |
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# IO Power Domain Map

| IO Domain | IO Group | Support of IO Voltage | | Default Actual assigned IO Domain Voltage | | Notes |
|---|---|---|---|---|---|---|
| | | 1.8V | 3.3V | Net Name of Power Supply | Voltage | |
| PMUIO0 | ***GPIO0A*** | ✓ | ✓ | *VCC_1V8* | *1.8V* | |
| PMUIO1 | ***GPIO0BC*** | ✓ | ✓ | *VCC_3V3* | *3.3V* | |
| VCCIO1 | ***GPIO0CD/GPIO1A*** | ✓ | ✓ | *VCCIO_FLASH* | *1.8V* | *GPIO0_B3/FLASH_VOL_SEL pin defined as a set pin for VCCIO1.* |
| VCCIO2 | ***GPIO1AB*** | ✓ | ✓ | *VCCIO_SD* | *3.3V* | |
| VCCIO3 | ***GPIO1BCD*** | ✓ | ✓ | *VCC_1V8* | *1.8V* | |
| VCCIO4 | ***GPIO1D/GPIO2A*** | ✓ | ✓ | *VCC_1V8* | *1.8V* | |
| VCCIO5 | ***GPIO2ABCD/GPIO3A*** | ✓ | ✓ | *VCC_3V3* | *3.3V* | |
| VCCIO6 | ***GPIO3ABC*** | ✓ | ✓ | *VCC_1V8* | *1.8V* | |
| VCCIO7 | ***GPIO3D/GPIO4A*** | ✓ | ✓ | *VCC_3V3* | *3.3V* | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |

# Power

U1000N
RV1126
BGA409 14R00X14R00X0R90

NPU/LOGIC/VEPU/ARM Power

| | | |
|---|---|---|
| NPU_VDD_1 | H11 | VDD_NPU_VEPU |
| NPU_VDD_2 | H12 | |
| NPU_VDD_3 | J10 | |
| NPU_VDD_4 | J11 | |
| NPU_VDD_5 | K10 | |
| NPU_VDD_6 | K11 | |
| LOGIC_VDD_1 | H9 | VDD_NPU_VEPU |
| LOGIC_VDD_2 | J9 | |
| LOGIC_VDD_3 | L10 | |
| LOGIC_VDD_4 | M11 | |
| LOGIC_VDD_5 | H13 | |
| LOGIC_VDD_6 | J13 | |
| VEPU_VDD_1 | L9 | VDD_NPU_VEPU |
| VEPU_VDD_2 | M9 | |
| VEPU_VDD_3 | N8 | |
| VEPU_VDD_4 | N9 | |
| ARM_VDD_1 | N12 | VDD_ARM |
| ARM_VDD_2 | P12 | |
| ARM_VDD_3 | P13 | |

Supply for VCCIO1~7 Power

VCCIO_VDD_1V8 — H14 — R7310 3.3R R0402 1% — VCC_1V8

C1000 1nF X5R 25V C0201

NOTE:
If any power domain of vccio 1 ~ vccio 7 is used,
then VCCIO_ VDD_ 1V8 must be connected to 1.8V power supply

VDD_NPU_VEPU

C1006 10uF X5R 4V C0402
C1005 1uF X5R 6.3V C0402
C1004 1uF X5R 6.3V C0402
C1001 100nF X5R 6.3V C0201

For NPU Power

VDD_NPU_VEPU

C1019 10uF X5R 4V C0402
C1018 1uF X5R 6.3V C0402
C1017 100nF X5R 6.3V C0201
C1016 100nF X5R 6.3V C0201

For VEPU Power

VDD_ARM

C1015 10uF X5R 4V C0402
C1014 1uF X5R 6.3V C0402
C1013 100nF X5R 6.3V C0201
C1012 100nF X5R 6.3V C0201

VDD_NPU_VEPU

C1011 10uF X5R 4V C0402
C1009 1uF X5R 6.3V C0402
C1010 1uF X5R 6.3V C0402
C1007 100nF X5R 6.3V C0201
C1008 100nF X5R 6.3V C0201

# GND

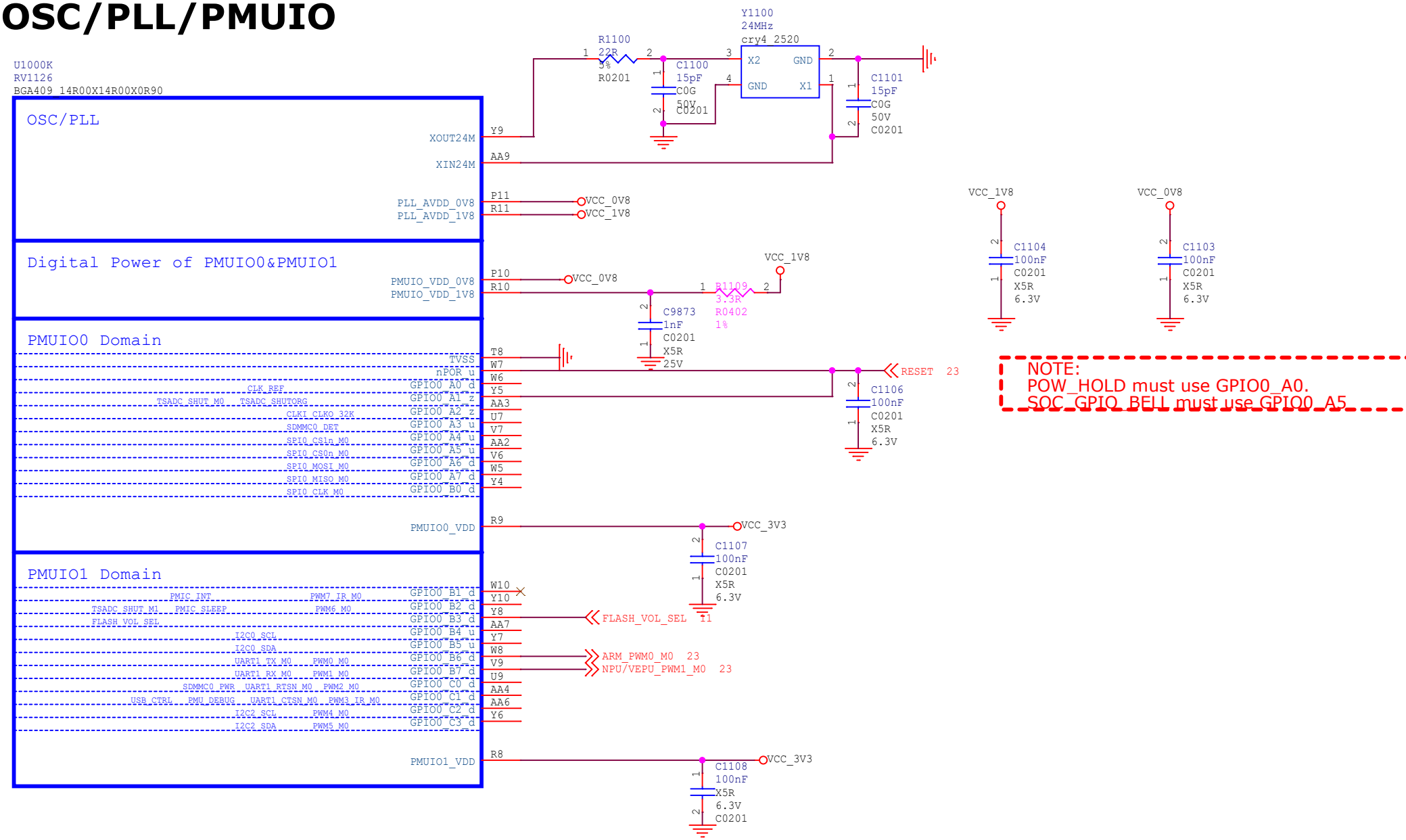
U1000O
RV1126
BGA409 14R00X14R00X0R90

VSS/AVSS

| | | | | | |
|---|---|---|---|---|---|
| A1 | VSS_1 | VSS_53 | K9 | | |
| A21 | AVSS_2 | VSS_54 | K12 | | |
| B12 | VSS_3 | VSS_55 | K13 | | |
| C3 | VSS_4 | VSS_56 | K14 | | |
| C5 | VSS_5 | VSS_57 | L2 | | |
| C7 | VSS_6 | VSS_58 | L5 | | |
| C10 | VSS_7 | VSS_59 | L6 | | |
| C12 | VSS_8 | VSS_60 | L11 | | |
| D9 | VSS_9 | VSS_61 | L12 | | |
| D12 | VSS_10 | VSS_62 | L13 | | |
| D18 | AVSS_11 | VSS_63 | L14 | | |
| E4 | VSS_12 | VSS_64 | L16 | | |
| E6 | VSS_13 | VSS_65 | M3 | | |
| E8 | VSS_14 | VSS_66 | M5 | | |
| E9 | VSS_15 | VSS_67 | M7 | | |
| E10 | VSS_16 | VSS_68 | M8 | | |
| E11 | VSS_17 | VSS_69 | M10 | | |
| E12 | VSS_18 | VSS_70 | M12 | | |
| F3 | VSS_19 | VSS_71 | M13 | | |
| F5 | VSS_20 | VSS_72 | M14 | | |
| F7 | VSS_21 | VSS_73 | M16 | | |
| F8 | VSS_22 | VSS_74 | N5 | | |
| F9 | VSS_23 | VSS_75 | N6 | | |
| F10 | VSS_24 | VSS_76 | N7 | | |
| F11 | VSS_25 | VSS_77 | N10 | | |
| F12 | VSS_26 | VSS_78 | N11 | | |
| F13 | VSS_27 | VSS_79 | N13 | | |
| F14 | AVSS_28 | VSS_80 | N14 | | |
| F15 | AVSS_29 | VSS_81 | N16 | | |
| G2 | VSS_30 | VSS_82 | P5 | | |
| G5 | VSS_31 | VSS_83 | P7 | | |
| G6 | VSS_32 | VSS_84 | P8 | | |
| G10 | VSS_33 | VSS_85 | P9 | | |
| G11 | VSS_34 | VSS_86 | P14 | | |
| G12 | VSS_35 | VSS_87 | P16 | | |
| G13 | VSS_36 | VSS_88 | R1 | | |
| G16 | AVSS_37 | VSS_89 | R5 | | |
| G17 | AVSS_38 | VSS_90 | R12 | | |
| H4 | VSS_39 | VSS_91 | R13 | | |
| H5 | VSS_40 | VSS_92 | R14 | | |
| H6 | VSS_41 | VSS_93 | T6 | | |
| H7 | VSS_42 | VSS_94 | T9 | | |
| H10 | VSS_43 | VSS_95 | T10 | | |
| H15 | VSS_44 | VSS_96 | T14 | | |
| J5 | VSS_45 | VSS_97 | T17 | | |
| J6 | VSS_46 | VSS_98 | V17 | | |
| J12 | VSS_47 | VSS_99 | W9 | | |
| J14 | VSS_48 | VSS_100 | W14 | | |
| J16 | VSS_49 | VSS_101 | AA1 | | |
| K5 | VSS_50 | VSS_102 | AA10 | | |
| K6 | VSS_51 | VSS_103 | AA21 | | |
| K8 | VSS_52 | | | | |

| | | | | | |
|---|---|---|---|---|---|
| Rockchip 瑞芯微电子 | Rockchip Electronics Co., Ltd | | | | |
| Project: | RV1126_REF | | | | |
| File: | 10.RV1126/1109_Power/GND | | | | |
| Date: | Tuesday, September 26, 2023 | | | Rev: | V1.1 |
| Designed by: | Yanhong.Li | Reviewed by: | <Checker> | Sheet: | 8 of 34 |

# OSC/PLL/PMUIO




NOTE:
POW_HOLD must use GPIO0_A0.
SOC_GPIO_BELL must use GPIO0_A5

NOTE:
The power domain configuration of GPIO should match the actual power supply.

| | | | | | |
|---|---|---|---|---|---|
| Rockchip 瑞芯微电子 | Rockchip Electronics Co., Ltd | | | | |
| Project: | RV1126_REF | | | | |
| File: | 11.RV1126/1109_OSC/PLL/PMUIO | | | | |
| Date: | Tuesday, September 26, 2023 | | | Rev: | V1.1 |
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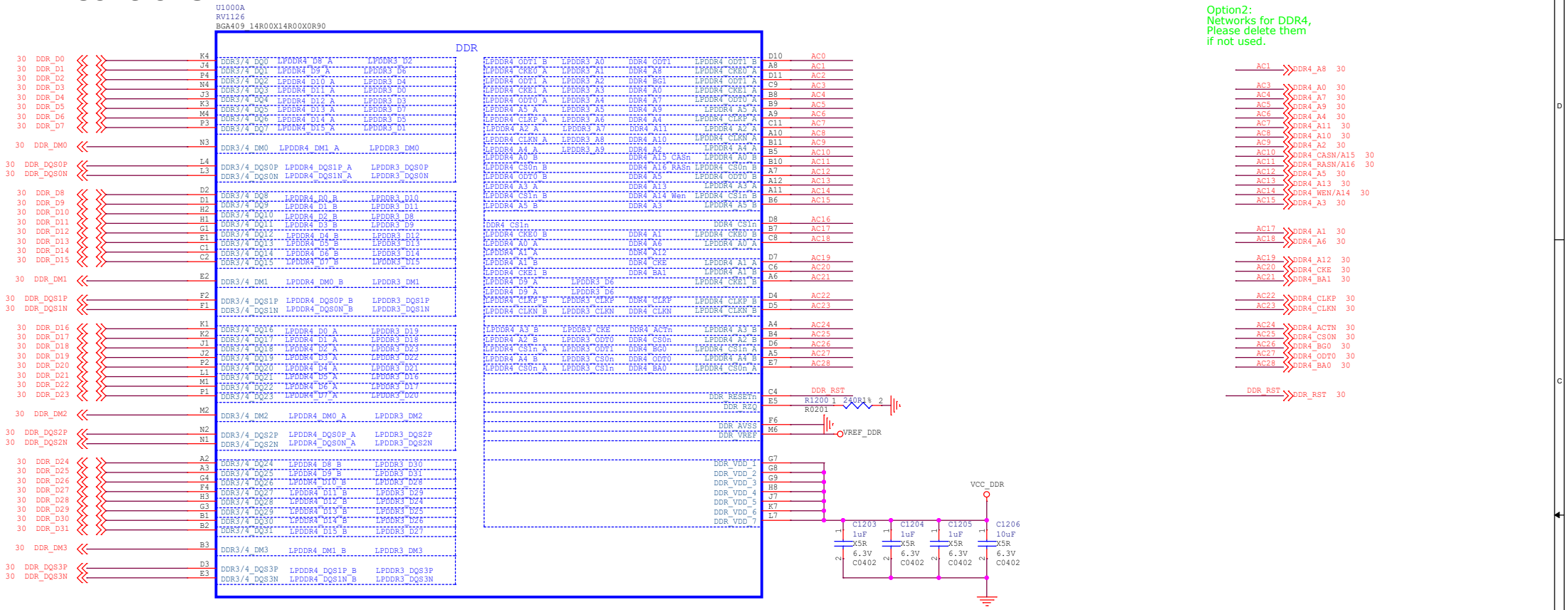
# DDR Controller




| | |
|---|---|
| Rockchip 瑞芯微电子 | Rockchip Electronics Co., Ltd |
| Project: | RV1126_REF |
| File: | 12.RV1126/1109_DRAM Controller |
| Date: | Tuesday, September 26, 2023 |
| Rev: | V1.1 |
| Designed by: | Yanhong.Li |
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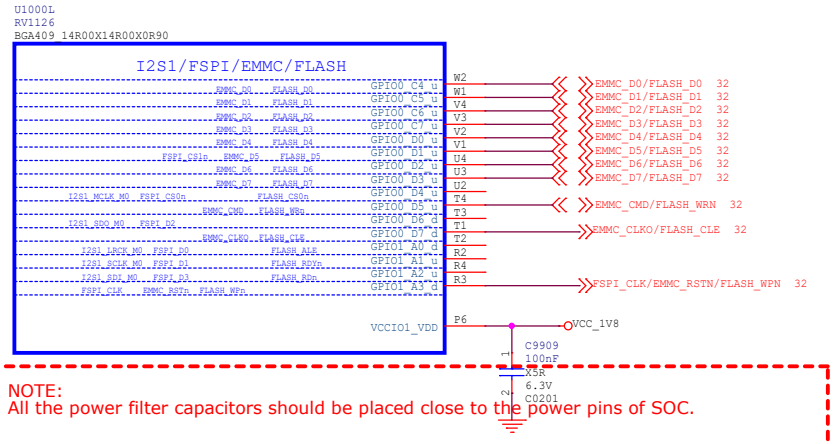
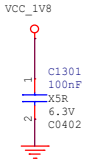
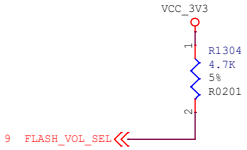
# EMMC/FLASH




NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.

NOTE:
The power domain configuration of GPIO should match the actual power supply.

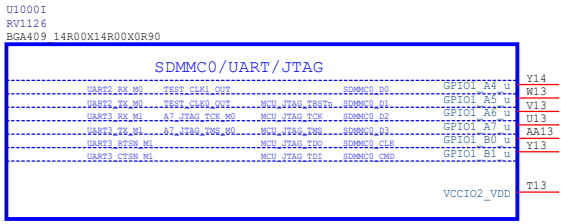



NOTE:
FLASH(VCCIO1) power domain IO supply configuration pin:

| Condition | VCCIO1 (VCCIO_FLASH) |
|---|---|
| FLASH_VOL_SEL=0 | 3.3V |
| FLASH_VOL_SEL=1 | 1.8V Default |

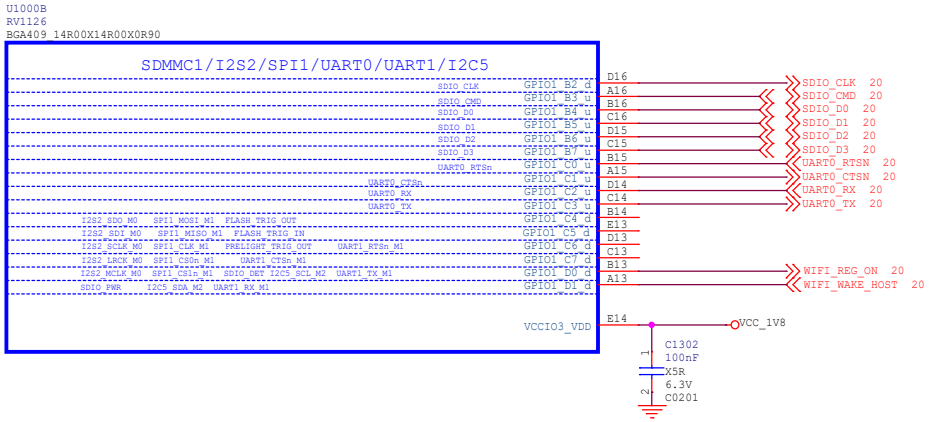
# SDMMC0/JTAG




NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.
If SD card is not used,please reserve MCU JTAG interface

NOTE:
The power domain configuration of GPIO should match the actual power supply.

# SDMMC1/UART/I2S2




NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.

NOTE:
The power domain configuration of GPIO should match the actual power supply.

| | | | | | |
|---|---|---|---|---|---|
| Rockchip 瑞芯微电子 | Rockchip Electronics Co., Ltd | | | | |
| Project: | RV1126_REF | | | | |
| File: | 13.RV1126/1109_Flash/SD | | | | |
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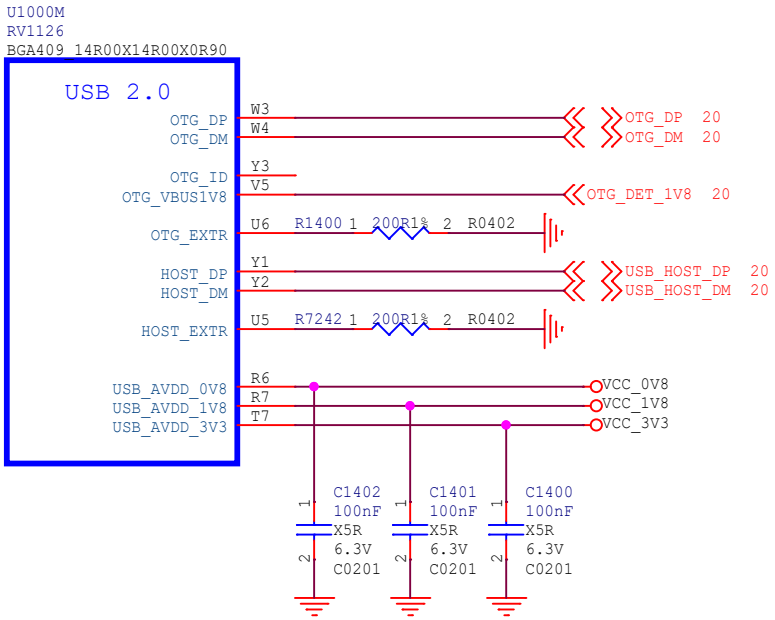
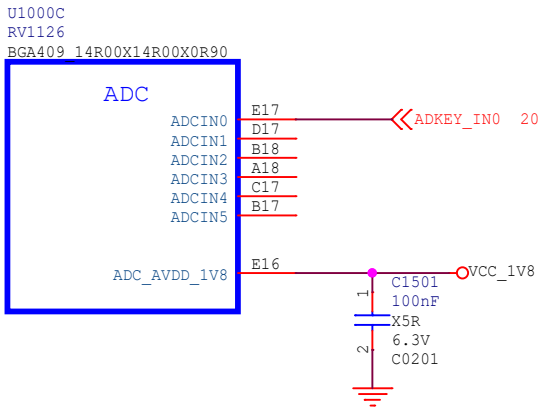
# USB Controller

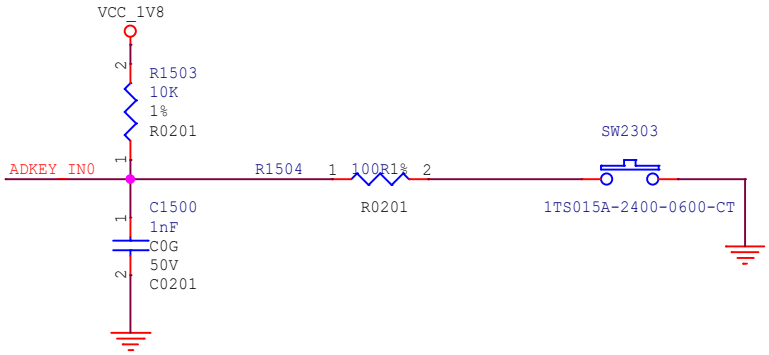



USB2.0 design rules:
1. Max intra-pair skew <4ps
2. Max trace length<6inchs
3. Max allowed via <6
4. Trace impedance 90ohm+/-10%
5. The distance between other signals follows the 3W rule.

| | | | | | |
|---|---|---|---|---|---|
| Rockchip 瑞芯微电子 | Rockchip Electronics Co., Ltd | | | | |
| Project: | RV1126_REF | | | | |
| File: | 14.RV1126/1109_USB Controller | | | | |
| Date: | Tuesday, September 26, 2023 | | | Rev: | V1.1 |
| Designed by: | Yanhong.Li | Reviewed by: | <Checker> | Sheet: | 12 of 34 |

# SARADC




| | | | | | |
|---|---|---|---|---|---|
| Rockchip 瑞芯微电子 | Rockchip Electronics Co., Ltd | | | | |
| Project: | RV1126_REF | | | | |
| File: | 15.RV1126/1109_SARADC | | | | |
| Date: | Tuesday, September 26, 2023 | | | Rev: | V1.1 |
| Designed by: | Yanhong.Li | Reviewed by: | <Checker> | Sheet: | 13 of 34 |

# CIF Interface


| | |
|---|---|
| BT1120 RX | DATA:CIF_DATA[15:0]<br>Y[0:7]:CIF_DATA[8:15]<br>Cb[0:7]:CIF_DATA[0:7]<br>CLOCK:CIF_CLKIN |
| 12bit CIF camera | CameraCIF[12:0]:CIF_DATA[15:4]<br>XCLK:CIF_CLKOUT<br>PCLK:CIF_CLKIN<br>HSYNC:CIF_HSYNC<br>VSYNC:CIF_VSYNC |
| 10bit CIF camera | CameraCIF[10:0]:CIF_DATA[15:6]<br>XCLK:CIF_CLKOUT<br>PCLK:CIF_CLKIN<br>HSYNC:CIF_HSYNC<br>VSYNC:CIF_VSYNC |
| 8bit CIF camera | CameraCIF[8:0]:CIF_DATA[15:8]<br>XCLK:CIF_CLKOUT<br>PCLK:CIF_CLKIN<br>HSYNC:CIF_HSYNC<br>VSYNC:CIF_VSYNC |

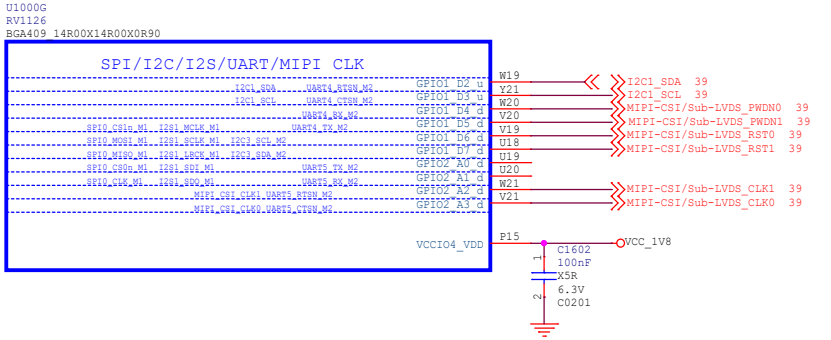
NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.

NOTE:
The power domain configuration of GPIO should match the actual power supply.

# MIPI-CSI Interface

MIPI_CSI_RX0 and MIPI_CSI_RX1 power pins are adjacent, so they share a decoupling capacitor
All the power filter capacitors should be placed close to the power pins of SOC.


# I2C/SPI/MIPI-CLK

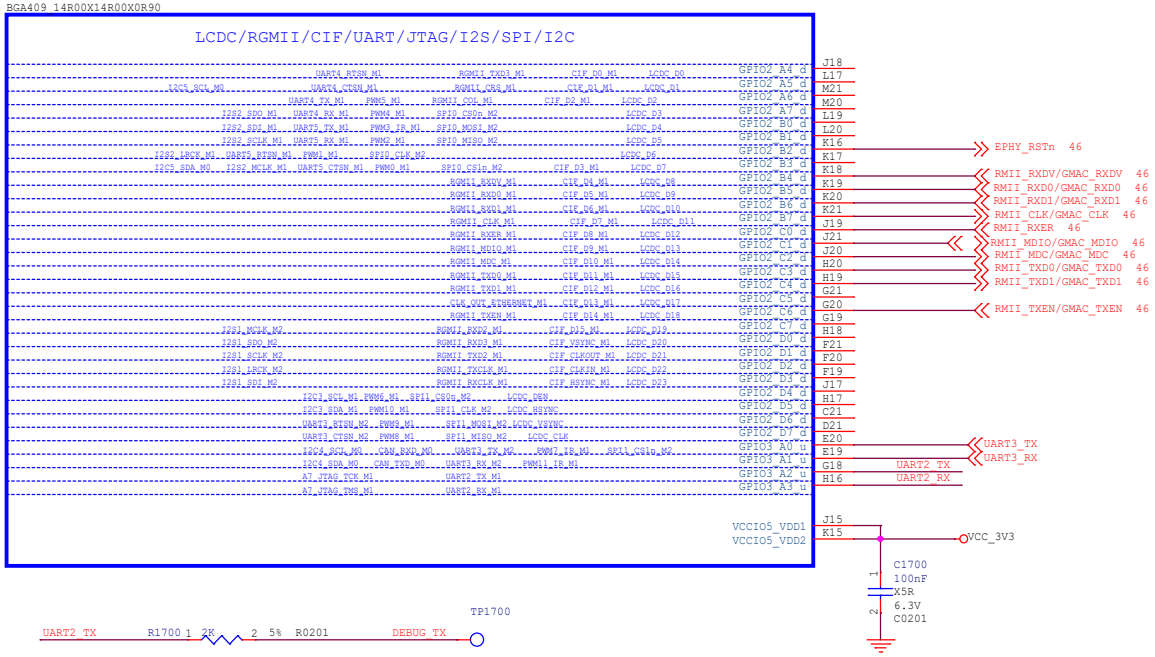


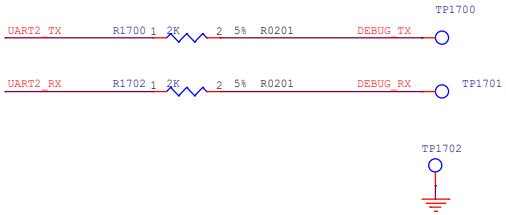

NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.

NOTE:
The power domain configuration of GPIO should match the actual power supply.

| | | | | | |
|---|---|---|---|---|---|
| Rockchip 瑞芯微电子 | Rockchip Electronics Co., Ltd | | | | |
| Project: | RV1126_REF | | | | |
| File: | 16.RV1126/1109_VideoInput | | | | |
| Date: | Tuesday, September 26, 2023 | | | Rev: | V1.1 |
| Designed by: | Yanhong.Li | Reviewed by: | <Checker> | Sheet: | 14 of 34 |

# LCDC/RGMII/PWM



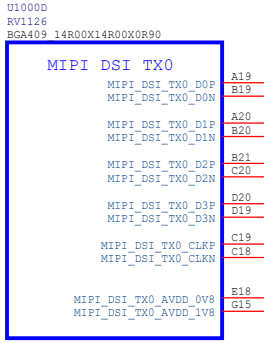




| | |
|---|---|
| BT1120 TX | DATA:LCDC_DATA[15:0]<br>Y[0:7]:LCDC_DATA[8:15]<br>Cb[0:7]:LCDC_DATA[0:7]<br>CLOCK:LCDC_CLK |
| 6bit Serial RGB | DATA:LCDC_DATA[5:0]<br>CLOCK:LCDC_CLK<br>HSYNC:LCDC_HSYNC<br>VSYNC:LCDC_VSYNC<br>DE:LCDC_DEN |
| 8bit Serial RGB | DATA:LCDC_DATA[7:0]<br>CLOCK:LCDC_CLK<br>HSYNC:LCDC_HSYNC<br>VSYNC:LCDC_VSYNC<br>DE:LCDC_DEN |
| 16bit Parallel RGB(RGB656) | R[4:0]:LCDC_DATA[15:11]<br>G[5:0]:LCDC_DATA[10:5]<br>B[4:0]:LCDC_DATA[4:0]<br>CLOCK:LCDC_CLK<br>HSYNC:LCDC_HSYNC<br>VSYNC:LCDC_VSYNC<br>DE:LCDC_DEN |
| 18bit Parallel RGB(RGB666) | R[5:0]:LCDC_DATA[17:12]<br>G[5:0]:LCDC_DATA[11:6]<br>B[5:0]:LCDC_DATA[5:0]<br>CLOCK:LCDC_CLK<br>HSYNC:LCDC_HSYNC<br>VSYNC:LCDC_VSYNC<br>DE:LCDC_DEN |
| 24bit Parallel RGB(RGB888) | R[7:0]:LCDC_DATA[23:16]<br>G[7:0]:LCDC_DATA[15:8]<br>B[7:0]:LCDC_DATA[7:0]<br>CLOCK:LCDC_CLK<br>HSYNC:LCDC_HSYNC<br>VSYNC:LCDC_VSYNC<br>DE:LCDC_DEN |

NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.

NOTE:
The power domain configuration of GPIO should match the actual power supply.

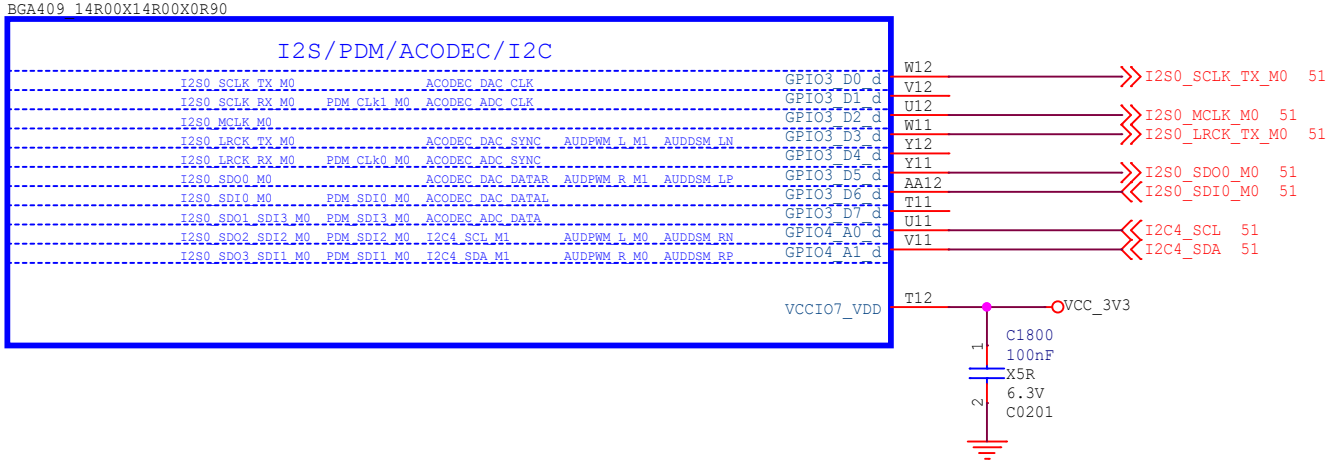
# MIPI-DSI Interface




| | | | | | |
|---|---|---|---|---|---|
| Rockchip 瑞芯微电子 | Rockchip Electronics Co., Ltd | | | | |
| Project: | RV1126_REF | | | | |
| File: | 17.RV1126/1109_VideoOutput Interface | | | | |
| Date: | Tuesday, September 26, 2023 | | | Rev: | V1.1 |
| Designed by: | Yanhong.Li | Reviewed by: | <Checker> | Sheet: | 15 of 34 |

# Audio Interface

U1000J
RV1126
BGA409_14R00X14R00X0R90



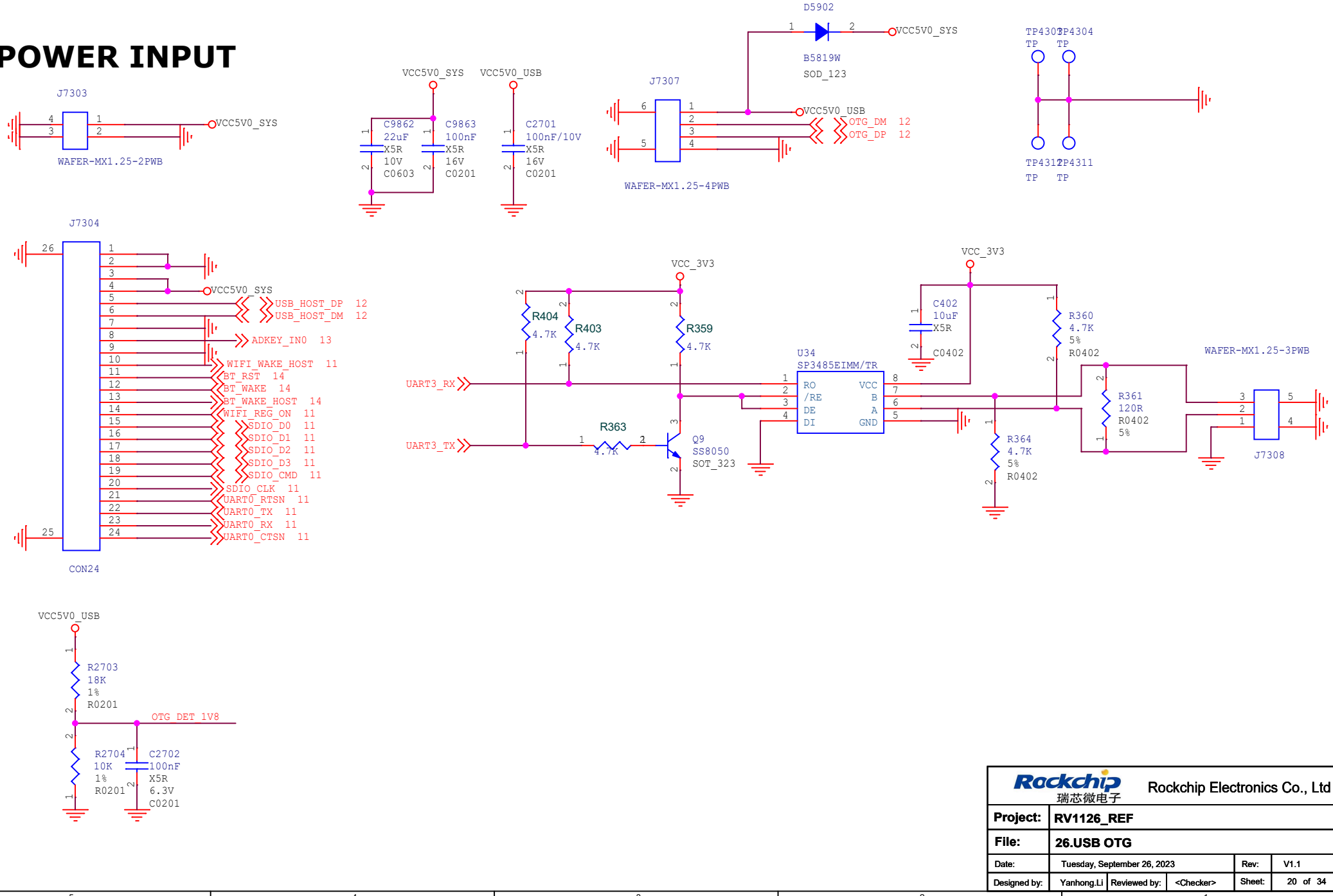

NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.

NOTE:
The power domain configuration of GPIO should match the actual power supply.

| | | | | | |
|---|---|---|---|---|---|
| Rockchip 瑞芯微电子 | Rockchip Electronics Co., Ltd | | | | |
| Project: | RV1126_REF | | | | |
| File: | 18.RV1126/1109_Audio | | | | |
| Date: | Tuesday, September 26, 2023 | | | Rev: | V1.1 |
| Designed by: | Yanhong.Li | Reviewed by: | <Checker> | Sheet: | 16 of 34 |

12 OTG_DET_1V8

# POWER INPUT

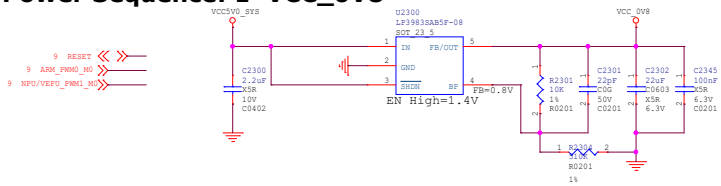



| | | | | | |
|---|---|---|---|---|---|
| Rockchip 瑞芯微电子 | Rockchip Electronics Co., Ltd | | | | |
| Project: | RV1126_REF | | | | |
| File: | 26.USB OTG | | | | |
| Date: | Tuesday, September 26, 2023 | | | Rev: | V1.1 |
| Designed by: | Yanhong.Li | Reviewed by: | <Checker> | Sheet: | 20 of 34 |

# Discrete Power

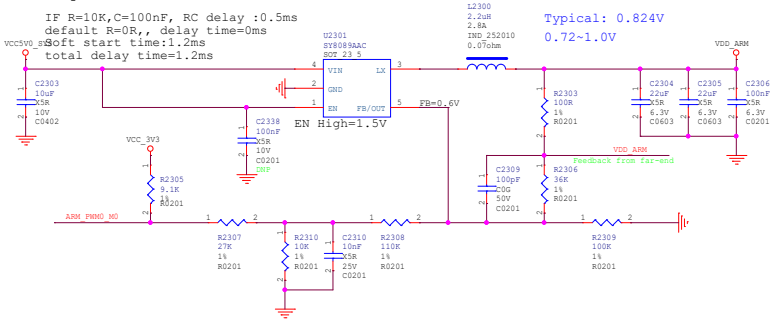
Discrete power supply is recommended for the following solutions:
1) Less peripheral equipment and less power supply
2) Small PCB space
3) The following discrete power supply solutions can reduce some devices according to the actual products,
Please read the notes on the power supply below.

## Power Sequence: 1 VCC_0V8



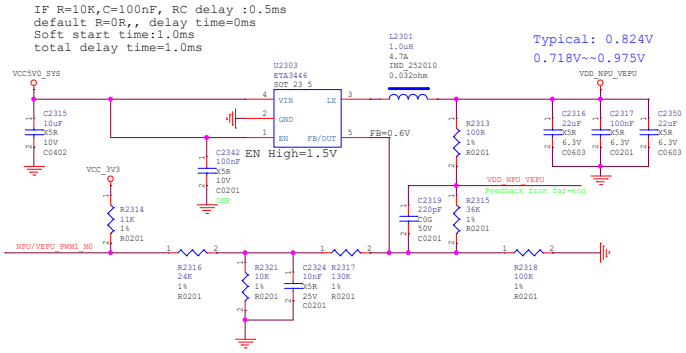

## Power Sequence: 2 VDD_LOGIC

## Power Sequence: 2 VDD_ARM




## Power Sequence: 2 VDD_NPU_VEPU

NOTE:
Recommend ETA3446 for better ripple.

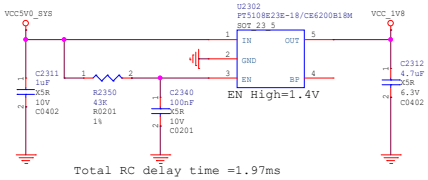



| VDD_LOG/NPU/VEPU power supply selection | R2314 | R2316 | R2317 | R2360 | Voltage range | NOTE |
|---|---|---|---|---|---|---|
| VDD_LOG/NPU/VEPU three-way merge | 24K | 12K | 330K | 0R | 0.72V~0.88V | (1) |
| only VDD_NPU_VEPU is powered together | 11K | 24K | 130K | NC | 0.715V~0.975V | (2) |

NOTE:
(1) Logic is combined with NPU and vepu:
the maximum voltage is only 0.88v, which makes the frequency of NPU not run very high.
It is only suitable for rv1109 and rv1126 without NPU high performance.

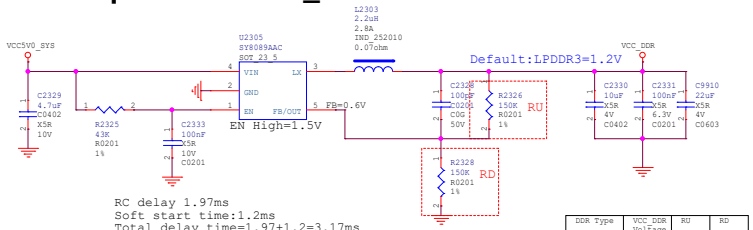
(2) Only NPU is combined with vepu:
It is only suitable for rv1109 and rv1126 .

## Power Sequence: 3 VCC_1V8




Total RC delay time =1.97ms

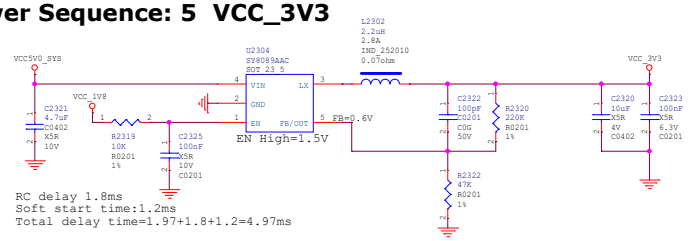
## Power Sequence: 4 VCC_DDR



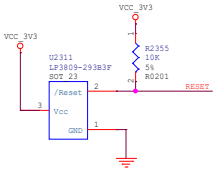

RC delay 1.97ms
Soft start time:1.2ms
Total delay time=1.97+1.2=3.17ms

| DDR Type | VCC_DDR Voltage | RU | RD |
|---|---|---|---|
| DDR3L | 1.35V | 150K | 120K |
| DDR3 | 1.5V | 150K | 100K |
| DDR4 | 1.2V | 150K | 150K |
| LPDDR3 | 1.2V | 150K | 150K |
| LPDDR4 | 1.1V | 150K | 180K |

## Power Sequence: 5 VCC_3V3




RC delay 1.8ms
Soft start time:1.2ms
Total delay time=1.97+1.8+1.2=4.97ms



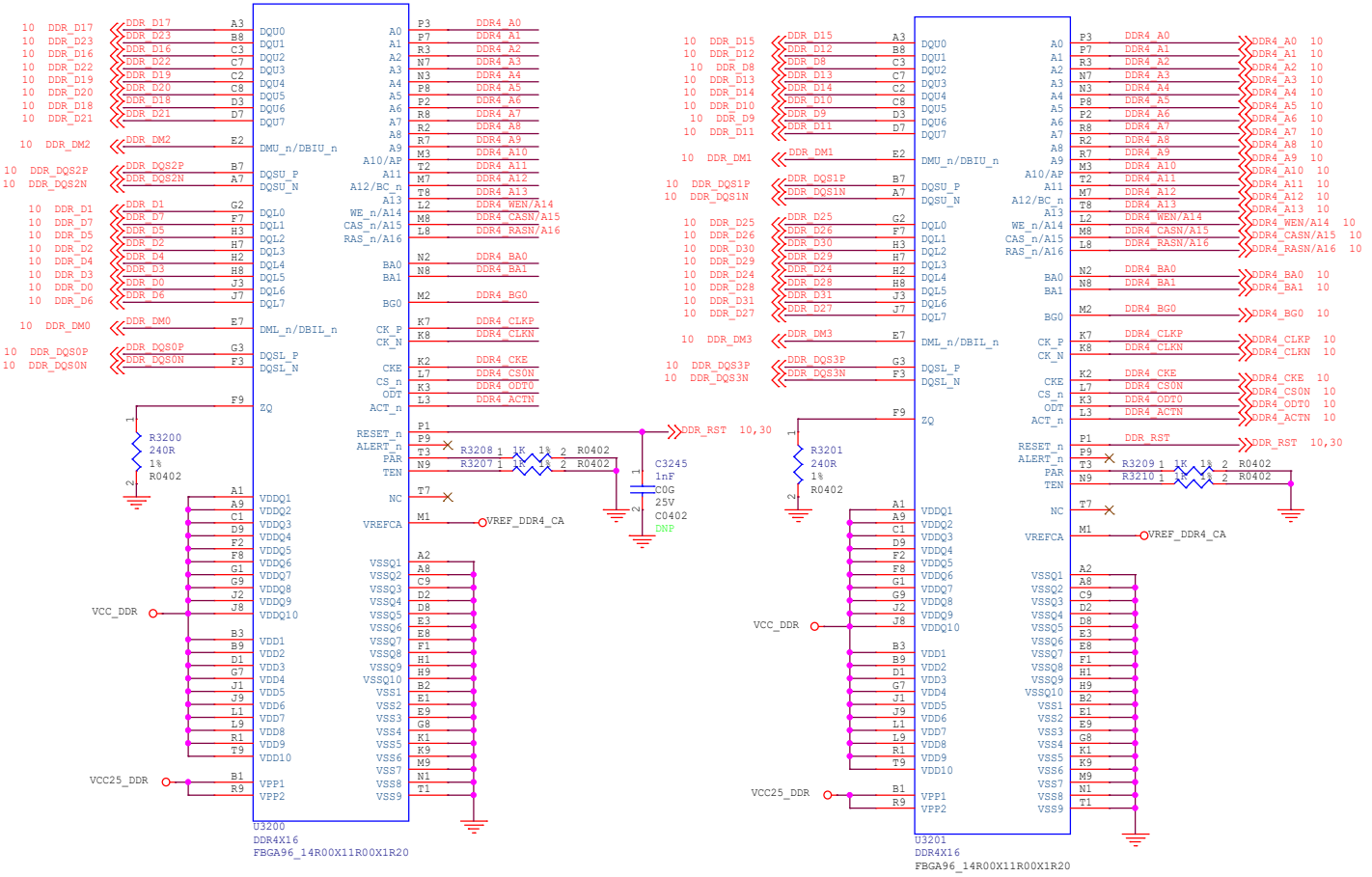

If you use a discrete solution, the power supply can be connected directly and the resistance can be removed.

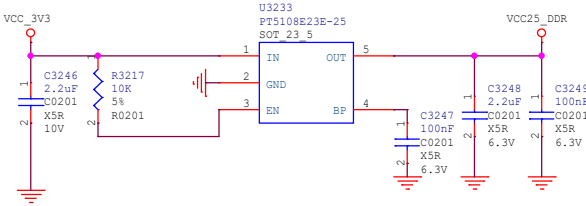
| | |
|---|---|
| Rockchip 瑞芯微电子 | Rockchip Electronics Co., Ltd |
| Project: | RV1126_REF |
| File: | 23.Discrete Power for System |
| Date: | Tuesday, September 26, 2023 |
| Rev: | V1.3 |
| Designed by: | Yanhong.Li |
| Reviewed by: | <Checker> |
| Sheet: | 23 of 54 |

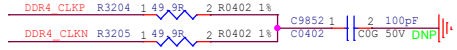
# DDR4 2x16bit

NOTE:
The sequence of DQ shall be done according to the template and shall not be adjusted or changed
Refer to the latest AVL for parts selection.

Note:
This is DDR template<RV1126_RV1109_Template_DDR4P216DD6_V10_20200325>.Six layers PCB.
If only need one pcs DDR, please must use U3200(lane0,lane2).

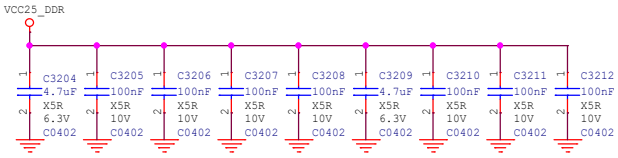


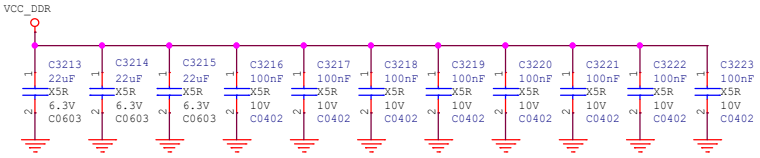



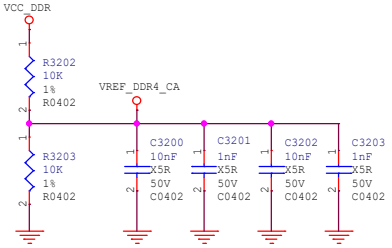



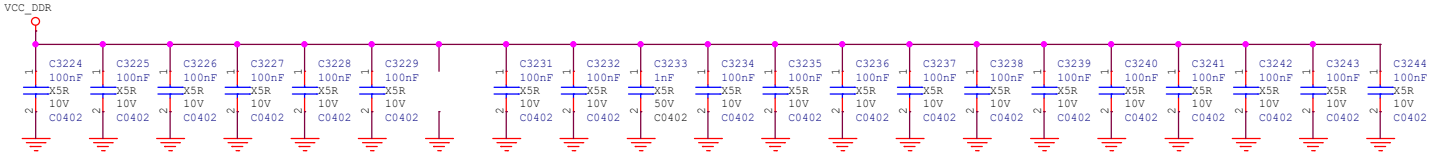






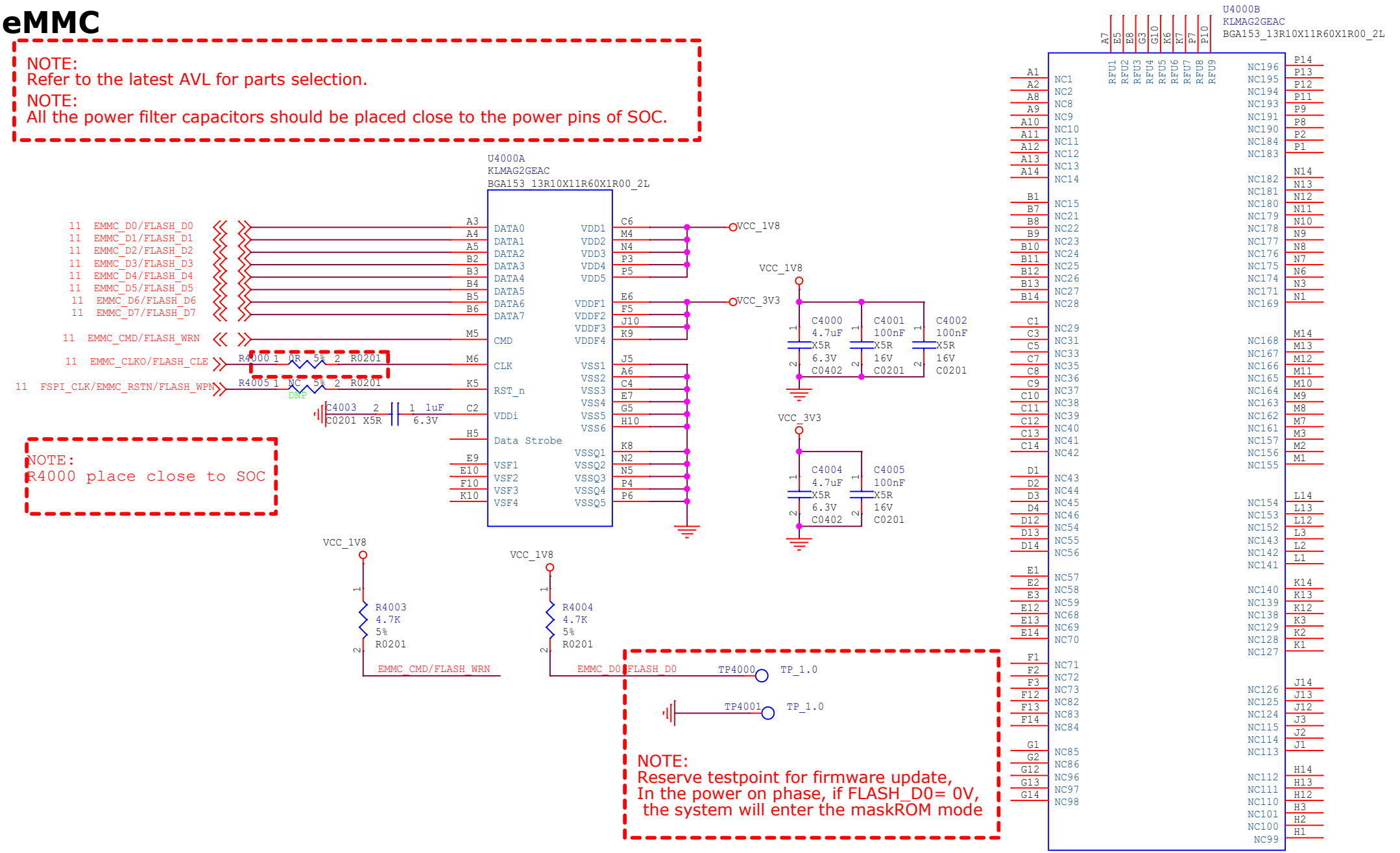




| | | | | | |
|---|---|---|---|---|---|
| Rockchip 瑞芯微电子 | Rockchip Electronics Co., Ltd | | | | |
| Project: | RV1126_REF | | | | |
| File: | 31. DRAM_LPDDR3_32 bit | | | | |
| Date: | Tuesday, September 26, 2023 | | | Rev: | V1.3 |
| Designed by: | Yanhong.Li | Reviewed by: | <Checker> | Sheet: | 30 of 54 |

# eMMC

NOTE:
Refer to the latest AVL for parts selection.
NOTE:
All the power filter capacitors should be placed close to the power pins of SOC.




NOTE:
R4000 place close to SOC

NOTE:
Reserve testpoint for firmware update,
In the power on phase, if FLASH_D0= 0V,
the system will enter the maskROM mode

| | | | | | |
|---|---|---|---|---|---|
| Rockchip 瑞芯微电子 | Rockchip Electronics Co., Ltd | | | | |
| Project: | RV1126_REF | | | | |
| File: | 40.Flash-eMMC Flash | | | | |
| Date: | Tuesday, September 26, 2023 | | | Rev: | V1.3 |
| Designed by: | Yanhong.Li | Reviewed by: | <Checker> | Sheet: | 32 of 54 |

M9900
MARK

M9901
MARK

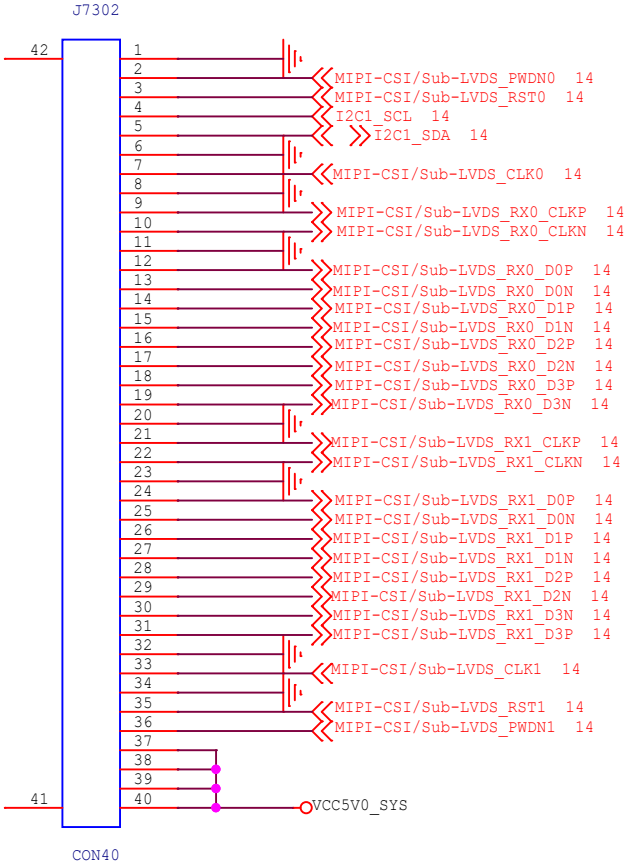
M9903
MARK

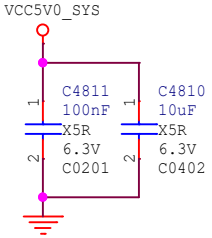
M9904
MARK

| | | | | | |
|---|---|---|---|---|---|
| Rockchip 瑞芯微电子 | Rockchip Electronics Co., Ltd | | | | |
| **Project:** | **RV1126_REF** | | | | |
| **File:** | **99.MARK/HOLE** | | | | |
| Date: | Tuesday, September 26, 2023 | | | Rev: | V1.1 |
| Designed by: | Yanhong.Li | Reviewed by: | <Checker> | Sheet: | 34 of 34 |

# Entrance Gate Solution

## 4 lane dual LVDS/MIPI Camera




| | | | | | |
|---|---|---|---|---|---|
| Rockchip 瑞芯微电子 | Rockchip Electronics Co., Ltd | | | | |
| Project: | RV1126_REF | | | | |
| File: | 48.Dual Sub-LVDS Camera(IR+RGB) | | | | |
| Date: | Tuesday, September 26, 2023 | | | Rev: | V1.3 |
| Designed by: | Yanhong.Li | Reviewed by: | <Checker> | Sheet: | 39 of 54 |

# PHY

15 RMII_TXD0/GMAC_TXD0
15 RMII_TXD1/GMAC_TXD1
15 RMII_TXEN/GMAC_TXEN
15 RMII_RXDV/GMAC_RXDV
15 RMII_RXER
15 RMII_RXD0/GMAC_RXD0
15 RMII_RXD1/GMAC_RXD1
15 RMII_MDIO/GMAC_MDIO
15 RMII_MDC/GMAC_MDC
15 RMII_CLK/GMAC_CLK
15 EPHY_RSTn

## PHY Address/LED

R6702 1 4.7K 5% 2 R0201 LED1/PHYAD1
VCC_3V3 R6704 1 4.7K 5% 2 R0201 LED0/PHYAD0

default
RMII_CLK/GMAC_CLK R6700 1 22R 5% 2 R0201 XTAL2
MAC-----> PHY

1. No crystal:
R6700,R6703,R6712, R6724 are sodered.
R6708,Y6700,C6702,C6703,R6717 are DNP.

2. With crystal
R6700,R6703,R6712, R6724 are DNP.
R6708,Y6700,C6702,C6703,R6717 are soldered.

## MII/RMII Selection

RXDV 1 R6722 4.7K 5% R0201 2 VCC_3V3

Pull High for RMII mode(default)

## WOL/LED0 Selection

RXD1 R6725 1 4.7K 2 5% R0201

Pull Low for LED0 Mode(default)
Pull High for WOL Mode
WOL:Wake-on-LAN

## UTP / Fiber Selection

RXER R6731 1 4.7K 2 5% R0201

Pull Low for UTP Mode(default)
Pull High for Fiber Mode

Close to CPU

RMII_TXD0/GMAC_TXD0 R6707 1 2 22R 5% R0201 TXD0
RMII_TXD1/GMAC_TXD1 R6710 1 2 22R 5% R0201 TXD1
RMII_TXEN/GMAC_TXEN TXEN

Close to PHY

RMII_RXD0/GMAC_RXD0 R6713 1 2 22R 5% R0201 RXD0
RMII_RXD1/GMAC_RXD1 R6714 1 2 22R 5% R0201 RXD1
RMII_RXDV/GMAC_RXDV CRS_DV
RMII_RXER RXER

EPHY_RSTn PHYRSTB
RMII_MDC/GMAC_MDC MDC
RMII_MDIO/GMAC_MDIO MDIO

## RMII REF_CLK direction

RMII_CLK_CTL R6712 4.7K 5% R0201 VCC_3V3

Pull Low for RMII REF_CLK Output mode
Pull High for RMII REF_CLK Input mode

This pin is pulled high by an external 4.7Kohm.
This pin is used for the interrupt function only when in the RMII mode.

RMII_INT R6720 4.7K 5% R0201 VCC_3V3

VCC_3V3
R6723 1.5K 5% R0201
R6724 10K 5% R0201
MDIO
TXD3

U6701
RTL8201F
QFN32_5R00X5R00X1R00_T

TXD0 TXC DVDD33 RXC RXD3/CLK_CTL RXD2/INTB RXD1 RXD0
TXD1 TXD2 TXD3 TXEN PHYRSTB MDC MDIO LED0/PHYAD0/PMEB
RXDV AVDD33_1 MDI1- MDI1+ MDI0- MDI0+ AVDD100UT RSET
LED1/PHYAD1 CRS/CRS_DV COL RXER/FXEN DVDD10OUT AVDD33_2 CRXTAI-OUT CRXTAI-IN E-Pad

R6735 4.7K 5% DNP PHYRSTB
C6722 100nF X5R 10V C0201
RTL8201F_RSET
DVDD10
VCC_3V3

Low-tension area

Differential mode lightning protection

High-tension area

Differential mode

U6702
TX0+ TX0- RX0+ RX0-
MS10232
TX+ TX- RX+ RX-
POE12 POE36
J7301
WAFER-MX1.25-6PWB

C6727 22nF C0402 X5R 25V
C6728 22nF C0402 X5R 25V
C6729 10nF X7R 100V C0402
C6730 10nF X7R 100V C0402
R6744 75R 1% R0805
R6743 75R 1% R0805
C9861 102/2KV C1206

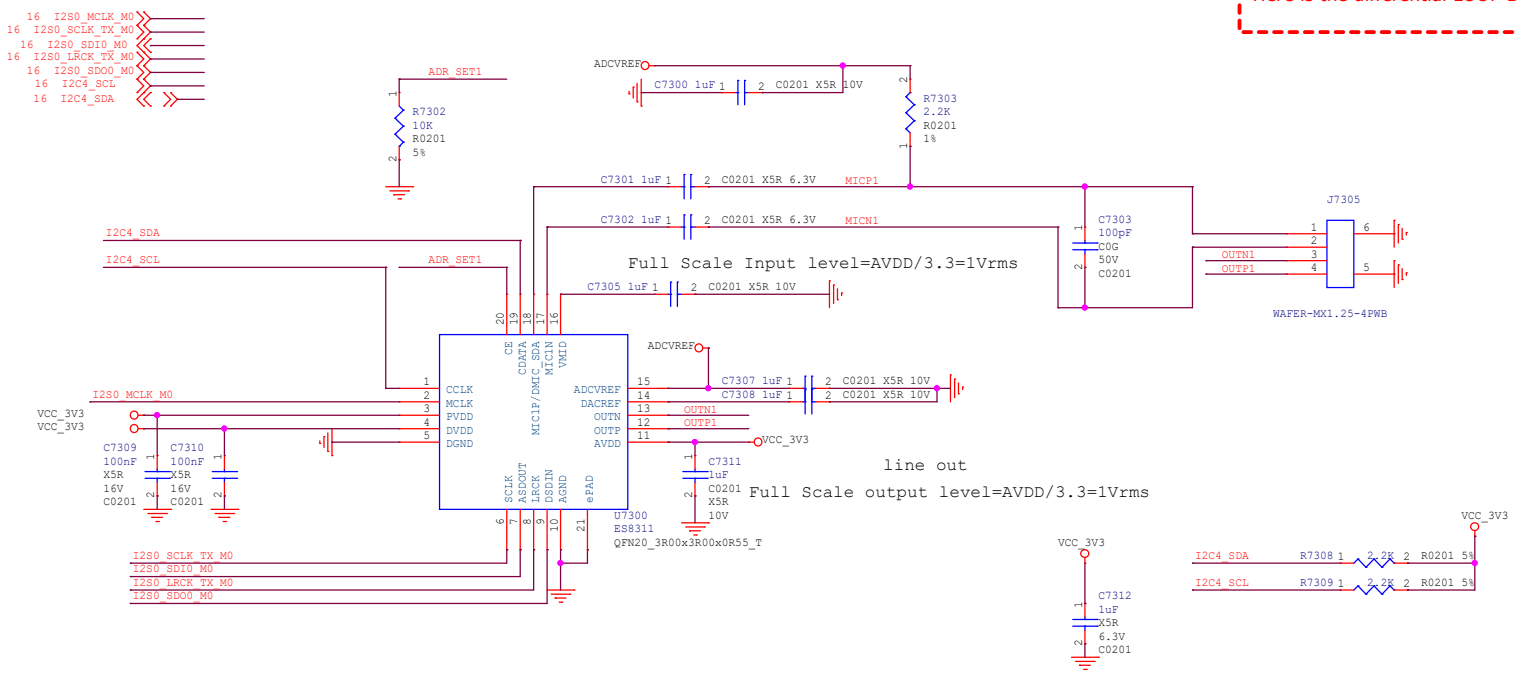
DVDD10 C6714 100nF X5R 10V C0201 close to PIN29
AVDD10 C6715 100nF X5R 10V C0201 close to PIN2
RTL8201F_RSET R6733 2.49K 1% R0201
VCC_3V3 C6716 4.7uF X5R 10V C0402
C6717 4.7uF C0402 X5R 10V
C6718 100nF C0201 X5R 16V close to PIN14
C6720 100nF C0201 X5R 16V
C6721 100nF C0201 X5R 16V close to PIN7,30

| | | | | | |
|---|---|---|---|---|---|
| Rockchip 瑞芯微电子 | Rockchip Electronics Co., Ltd | | | | |
| Project: | RV1126_REF | | | | |
| File: | 67.Ethernet-EPHY_RMII | | | | |
| Date: | Tuesday, September 26, 2023 | | | Rev: | V1.3 |
| Designed by: | Yanhong.Li | Reviewed by: | <Checker> | Sheet: | 46 of 54 |

# Audio3 for Discrete Power solution

NOTE: IO level=3.3V ,VCCIO7_VDD=3.3V

NOTE:
1. The MIC IN of ES8311 is recommended to use differential MIC.
2. There is a loopback funtion inside ES8311, so the hardware loopback circuit can be delected outside.
3. If the audio solution is changed, the loopback circuit will need to use.
Here is the differential LOOP BACK circuit fot reference.




| | | | | | |
|---|---|---|---|---|---|
| Rockchip 瑞芯微电子 | Rockchip Electronics Co., Ltd | | | | |
| Project: | RV1126_REF | | | | |
| File: | 73.Audio3(Discrete solution) | | | | |
| Date: | Tuesday, September 26, 2023 | | | Rev: | V1.3 |
| Designed by: | Yanhong.Li | Reviewed by: | <Checker> | Sheet: | 51 of 54 |